10-06-2023

Board of studies (BoS) Minutes of the Meeting

Minutes of Board of Studies (BoS) meeting of Electronics and Communication Engineering held at board room, A-block in hybrid mode at 10.00 A.M.

The zoom link is:
https://us02web.zoom.us/j/6400485257?pwd=jN9IMqLRUorw6gcZ3E5gmA-QPIBvN0.

Chairman BoS invited all the external and internal members.

Agenda of the meeting:

1. Syllabus discussion on new UG B.Tech in Electronics Engineering (VLSI Design and Technology)
2. Offering the above program to 2022 B.Tech ECE admitted students.
3. Revising the existing PG M.Tech VLSI program in accordance with R22 structure.
4. Introduction of new R22 PG M.Tech IoT program in Collaboration with Efftronics Systems Pvt. Ltd.
5. Few Modifications in existing R22 - B.Tech ECE (Addition of courses in Department Electives and Minors).
6. NPTEL Course list for approval.

The following external and internal members are attended for the meeting in hybrid mode.

External BoS members.

1) Dr. Sreehari Rao Patri, Professor & HoD, Department of ECE, National Institute of Technology, Warangal.
2) Dr. K. Krishna Naik, Associate Professor, Department of ECE, IIIT DM, Kurnool. (Online)
3) Dr. Narasimha Sarma N V S, Director, IIIT Trichy, Trichy. (Online)
4) Dr. K Subbarangaiah, Director, Veda IIT, Hyderabad. (Online)
5) Mr. Bhavani Shankar, Executive Manager & Head – IoT, Efftronics System Pvt Ltd, Vijayawada. (Online)

Internal BoS members.

1) Dr. T. Pitchaiah, Professor, HoD and BoS Chairman
2) Dr. N. Usha Rani, Professor & Dean, SEECE

3) Dr. B. Seetha Ramanjaneyelu, Professor and member
4) Dr. M. S. S. Rukmnini, Professor and member
5) Dr. SK. Jakeer Hussain, Professor & Dean, IPM (Online)
6) Dr. M. Sarada, Professor and member
7) Dr. Y. Ravi Sekhar, Professor and member
8) Dr. M. Pachiyanan, Associate Professor and member
9) Dr. K. Annapurna, Associate Professor and member
10) Dr. P. J. Reginald, Assistant Professor and member
11) Dr. G. Pradeep, Assistant Professor and member
12) Dr. Shard Kumar Tiwari, Assistant Professor and invited member
13) Dr. V. Vijaya Lakshmi, Assistant Professor and invited member
14) Dr. G. S. R. Satyanarayana, Assistant Professor and secretary

Agenda1 - Discussion

Dr. Sreehari Rao Patri:

1. Clarification asked regarding formative assessments and question bank preparation and its level. HoD, ECE clarified the above.
2. Suggested to push Network Theory into I year I semester if possible.
3. Suggested to include EMTL and Antenna concepts in the curriculum.
4. Use B. Tech ECE signals and systems course as it is.
5. Instructed to offer the course Probability and Stochastics Process in place of Probability and Statistics. Use "Probability, Random Variables, and Random Signal Principles" by Peebles as text book. The reference book can be "Probability, Random Variables and Stochastic Processes" by Unni Krishnanan.
6. Felt Analog Circuits-1 syllabus is heavy. Name up to class G and H amplifiers and their applications in brief.
7. Analog Circuits course can be of three parts as 1, 2, 3. The tuned amplifiers and power amplifiers can be offered as one course.
8. Suggested to drop the course VLSI Design, as much of the content is offered in the other similar courses, layout concepts have to be included in respective custom IC design subjects.

Dr. K. Krishna Naik:

1. Asked to correct Probability and statistics LTP structure.
2. DICA seems to be redundant, instead discuss analog and digital IC applications.
3. FPGA prerequisite subject can be placed instead of management science subject.
4. In Micro Electronic subject latest developing technologies such as nano wires can be included.

Dr. Narasimha Sarma N V S:

1. Suggested to introduce a "Design Thinking" course instead of advanced coding competency.
2. Numerical method concepts can be included rather than stochastic process later Dr. Sreehari Rao Patri justified the use of stochastic process.
3. If possible remove the Environmental studies and Life skill courses so that some of the important courses can be accommodated in the curriculum.
4. Suggested to offer Digital Logic Design and Signals and Systems courses as two parts.
5. Tabular minimization method should be included in DLD.
6. Unit-1 and Unit-4 of physics for electronic engineers can be removed, suggested to add thermodynamic concepts which will be useful to design the high-speed circuits.
7. Asked to include DC machines and transformer concepts in BEEE course. Mr. Bhavani Sankar has supported as industry mostly using brushless DC motors.
8. IT tools /workshop course content can be replaced with PCB lab, particularly for B.Tech electronics students.
9. Suggested to include MATLAB based books for PTSP course.
10. Felt that Analog Circuits -1 is heavy.
11. Suggested to offer a course on Data communications, Mr. Bhavani Sankar also raised this issue.

Dr. K Subbarangaiah:

1. Highlighted the necessity of OOPS concept for System Verilog course.
2. Asked to include bus concepts such as AMBA bus in SOC course.
3. Suggested to make ASIC as core course.
4. Suggested to offer RF transmission lines instead of EMTL course, impedance matching concepts need to be discussed in detailed manner.
5. In Physical Design and Automation course along with floor planning, power planning concepts needed to be added.
6. Suggested a proper flow for Physical Design and Automation, which as follows as standard cell libraries, simulation and logic synthesis, floor planning and power planning, physical verification with layout vs schematic, design for manufacturability.
7. Elaborate on LNA topologies in CMOS RF design course. Asked to swap the module 2 units.
8. For CMOS RF design use text book "RF Microelectronics" by Razavi.
9. In RFIC course elaboration of the following topics is required active passive matching and LNA.
10. Mixed signal design can be a core course and, lab component need to be added. Methods of testing for DAC and ADC can be added. Text book authored by Allen and Holberg.
11. In hardware security course concepts of encryption and physical isolation of logic has to be added.
12. Offer VLSI signal processing as honors and Digital Signal Processing course should be prerequisite for it.
13. Offer HW/SW codesign as early as possible

Mr. Bhavani Shankar:

1. Data structures and programming must be clubbed.
2. OOPS concepts can be included anywhere in curriculum.
3. Asked to offer DC machine concepts in BEEE.
4. Asked to adopt "Digital Designs: Principles And Practice" by John F. Wakerly as one of the text book.
5. Data communication concepts must be offered for VLSI design engineers as they are application area.

The resolutions made after Agenda 1 discussion are:

- To accommodate some of the courses BoS members suggested to incorporate minor modifications in curriculum structure where ever required.
- The chairman BoS agreed to incorporate the appropriate points in syllabi.
- All BoS members agreed to go with this programme. Members suggested to fix/freeze two years syllabus, and if required modifications can be done in later part of the program.

Agenda 2-Discussion

1. The members appreciated the initiative of offering the B.Tech in Electronics Engineering (VLSI Design and Technology) for 2022 admitted students. Dr. Sreehari Rao Patri and Dr. Narasimha Sarma N V S has cautioned about legal implications, and directed to take written concern from both parents and students.
2. If any issues arise due to first year gap they suggested to offer some bridge course.

The resolution made after Agenda 2 discussion is:

- Not to go with above plan as more legal implications might have to face and all BoS members agreed to that.

Agenda 3- Discussion

1. Dr. Subbarangaiah asked to to make FPGA as core course and Device modelling as elective.
2. He also suggested to add SPICE models in Device modelling.
3. Dr. Sreehari Rao Patri suggested to include the RTL concepts in digital IC design.
4. Verilog A can be offered as an elective course.

The resolution made after Agenda 3 discussion is:

- All members agreed the proposed structure with minor modifications, as some of the courses need to offer in first semester itself, and agreed to incorporate the appropriate points in the syllabi.

Agenda 4- Discussion

1. Dr. Krishna naik raised issue with logistics involved when student first goes to industry (i.e. Efftronics Pvt Ltd) and come back to VFSTR and back to industry. HoD ECE clarified that both VFSTR and Efftronics are in reasonable distance and not much logistic problem arises.
2. Dr. Narasimha Sarma N V S raised about approval issues and Mr. Bhavani sankar clarified that similar program was carried along with JNTU Anantapur.
3. Dr. Narasimha Sarma N V S asked to include some funding agency concepts in business system course.
4. Dr. Narasimha Sarma N V S suggested to conduct every semester a BoS meeting so that close monitoring of this program will happen.
5. Dr. Sreehari Rao Patri asked about the job offer at Efftronics and Mr. Bhavani sankar promised that all the candidates who performed well can get job at their facility.
6. Dr. Narasimha Sarma N V S cautioned about how first semester evaluation would take place and asked to derive some plan.

The resolution made after Agenda 4 discussion is:

- BoS members strongly agreed and recommended the M. Tech IoT program for the approval of academic council.

Agenda 5-Discussion

All the members anonymously agreed the presented AIML honors course content.

Agenda 6-Discussion

Dr. Narasimha Sarma N V S suggested to take feedback from the students after completion of the course and take appropriate actions.

The overall conclusion of the meeting is based on suggestions given by BoS members, the chairperson of BoS told that, those suggestions would be incorporated appropriately in the curriculum and syllabi and this would be recommended to Academic Council of VFSTR for the approval.

There being no further points for discussion, the chairperson thanked all the members and announced the meeting was adjourned.

Chairman BoS

Dr. T. Pitchaiah